

## sdmay23-47: CyDAQ DSP Platform Firmware and Software Redesign

Week 9 Report

November 28 - December 2

### Team Members

Blake Fisher — *GUI Engineer Lead*

Corbin Kems — *CLI Engineer Lead*

Wyatt Duberstein — *CLI Engineer*

Long Zeng — *Firmware Engineer Lead*

Cole Langner — *Testing Lead*

Yohan Bopearatchy — *Firmware Engineer*

Jens Rasmussen — *Project Lead*

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### Summary of Progress this Report

Software:

- Finished basic operation mode. Added connection status indicator. Improved GUI.

Hardware:

- Finished communication core basic operation. Started making tests and demos.

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### Pending Issues

Software:

- Connection status not completely working.

Hardware:

- Sampling producing weird binary characters.

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### Plans for Upcoming Reporting Period

Software:

- No immediate plans. Beginning next semester, we will work on support for the rest of the modes, improving the GUI, and live plotting.

Hardware:

- No immediate plans. Beginning next semester, we will work on core speeds and getting live plotting possible

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### Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Blake Fisher	GUI work	6	0
Corbin Kems	Finished the needed features for demo. Got connection status almost working	8	0
Wyatt Duberstein	Input validation	4	0

Long Zeng	Finished comm core basic operation, started making tests and demos	6	
Cole Langner	Looked into how to mock CLI/GUI for automated tests	2	0
Yohan Bopearatchy	Worked on getting cli communication with the firmware working	2	0
Jens Rasmussen	Design document work and prepared for demo.	4	

### Gitlab Activity Summary

#### Commit statistics for master Sep 20 - Dec 02

Excluding merge commits. Limited to 2,000 commits.

master

sdmay23-47

- Total: **156 commits**
- Average per day: **2.1 commits**
- Authors: **7**

Commits per day of month

